AMENDMENTS TO THE CLAIMS

Listing Of Claims

1. (currently amended) A semiconductor package comprising:

a substrate ~~having~~ comprising a first side, an opposing second side, a plurality of die contacts on the first side, and a plurality of bonding sites on the second side in electrical communication with the die contacts, each bonding site comprising an electrically conductive, bondable metal;

a semiconductor die on the ~~substrate~~ first side comprising a plurality of bond pads bonded to the die contacts; and

~~in electrical communication with the bonding sites;~~

a plurality of external contacts on the ~~bonding sites~~ second side, each external contact comprising a multi layered metal bump including a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing outer layer on the second metal layer.

~~; and~~

~~an encapsulant on the substrate encapsulating the die.~~

2. (currently amended) The semiconductor package of claim 1 ~~further comprising a plurality of die contacts on the substrate in electrical communication with the external contacts,~~ wherein the die contacts ~~comprising~~ comprise multi layer metal bumps.

~~bonded to the bond pads on the die.~~

3. (currently amended) The semiconductor package of claim 1 ~~further comprising a plurality of die contacts on the substrate in electrical communication with the external contacts, and~~ wherein the die is back bonded to the ~~substrate~~ first side and wire bonded to the die contacts.

4. (currently amended) The semiconductor package of claim 1 wherein the electrically conductive, bondable metal comprises copper, the first metal layer comprises copper, the second metal layer comprises nickel, and the non-oxidizing outer layer comprises gold.

5. (currently amended) The semiconductor package of claim 1 wherein the substrate comprises a material selected from the group consisting of ~~bismaleimide-trizine (BT),~~ organic polymer materials, epoxy resins, and polyimide resins.

6. (currently amended) The semiconductor package of claim 1 wherein the die is wire bonded to the ~~substrate~~ die contacts in a chip-on-board configuration.

7. (currently amended) The semiconductor package of claim 1 wherein the die is wire bonded to the ~~substrate~~ die contacts in a board-on-chip configuration.

8. (currently amended) The semiconductor package of claim 1 wherein the substrate includes a recess and the die is contained in the recess in contact with a metal heat spreader.

9. (currently amended) A semiconductor package comprising:

a substrate having a first side and an opposing second side;

~~comprising a board material;~~

a plurality of die contacts on the ~~substrate~~ first side in a pattern, and a plurality of external contacts on the ~~substrate~~ second side in an array in electrical communication with the die contacts, each die contact and each external contact comprising a multi layered metal bump

including a base metal layer, a bump metal layer and a non-oxidizing outer metal layer; and

a semiconductor die flip chip mounted to the ~~substrate~~ first side, the die comprising a plurality of bond pads in the pattern bonded to the die contacts.

10. (currently amended) The semiconductor package of claim 9 further comprising an encapsulant on the substrate encapsulating the die and the first side.

11. (previously presented) The semiconductor package of claim 9 wherein the base metal layer comprises copper, the bump metal layer comprises nickel, and the non-oxidizing outer metal layer comprises gold.

12. (previously presented) The semiconductor package of claim 9 wherein each die contact and each external contact is generally pyramidal in shape with a planar tip portion.

13. (currently amended) The semiconductor package of claim 9 further comprising a solder mask on the ~~substrate~~ second side configured to electrically insulate the external contacts.

14. (currently amended) A semiconductor package comprising:

a substrate having a first side, and an opposing second side;

a plurality of die contacts on the first side comprising first multi layered metal bumps in a pattern having generally planar first tip portions;

a plurality of bonding sites on the second side in an array in electrical communication with the die contacts, each bonding site comprising an electrically conductive, bondable metal;

a plurality of external contacts on the ~~second side~~ bonding sites in electrical communication with the die contacts comprising second multi layered metal bumps having generally planar second tip portions; and

a semiconductor die flip chip mounted to the substrate, the die comprising a plurality of bond pads in the pattern bonded to the die contacts.

15. (previously presented) The semiconductor package of claim 14 wherein each first multi layered metal bump and each second multi layered metal bump comprises a copper layer, a nickel layer and a gold layer.

16. (previously presented) The semiconductor package of claim 14 further comprising an encapsulant on the substrate encapsulating the die.

17. (currently amended) The semiconductor package of claim 14 wherein the bonding sites ~~die contacts have a pattern matching that of the bond pads on the die~~ and the external contacts are in a grid array.

18. (currently amended) A semiconductor package comprising:

a substrate having a first side and an opposing second side;

a plurality of die contacts on the first side;

a plurality of bonding sites on the second side in electrical communication with the die contacts, each bonding site comprising an electrically conductive, bondable metal;

a plurality of external contacts on the bonding sites, each external contact comprising a multi layered metal bump including a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing third metal layer on the second metal layer; and

a semiconductor die back bonded to the first side in a chip-on-board configuration, the die comprising a plurality of bond pads wire bonded to the die contacts.

19. (previously presented) The semiconductor package of claim 18 wherein the first metal layer comprises copper, the second metal layer comprises nickel and the non-oxidizing third metal layer comprises gold.

20. (previously presented) The semiconductor package of claim 18 further comprising an encapsulant on the substrate encapsulating the die.

21. (currently amended) The semiconductor package of claim 18 wherein the substrate comprises a material selected from the group consisting of ~~bismaleimide-trizine (BT),~~ organic polymer materials, epoxy resins, and polyimide resins.

22. (currently amended) A semiconductor package comprising:

a substrate having a first side, an opposing second side and an opening;

a plurality of bonding sites on the second side and a plurality of conductors on the second side in electrical communication with the bonding sites, each bonding site comprising an electrically conductive, bondable metal;

a plurality of external contacts on the bonding sites, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing third metal layer on the second metal layer; and

a semiconductor die bonded to the first side in a board-on-chip configuration, the die comprising a plurality of bond pads aligned with the opening and wire bonded to the conductors.

23. (previously presented) The semiconductor package of claim 22 wherein the first metal layer comprises copper, the second metal layer comprises nickel and the third metal layer comprises gold.

24. (previously presented) The semiconductor package of claim 22 further comprising an encapsulant on the substrate encapsulating the die.

25. (currently amended) The semiconductor package of claim 22 wherein the substrate comprises a material selected from the group consisting of ~~bismaleimide-trizine (BT),~~ organic materials, epoxy resins, and polyimide resins.

26. (currently amended) A semiconductor package comprising:

a substrate having a first side, an opposing second side and a recess;

a plurality of bonding sites on the second side and a plurality of conductors on the second side in electrical communication with the bonding site, each bonding site comprising an electrically conductive, bondable metal;

a plurality of external contacts on the bonding sites, each external contact comprising a multi layer metal bump including a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing third metal layer on the second metal layer;

a metal heat spreader in the recess; and

a semiconductor die in the recess in contact with the heat spreader, the die comprising a plurality of bond pads wire bonded to the conductors.

27. (previously presented) The semiconductor package of claim 26 further comprising an encapsulant in the recess encapsulating the die.

28. (previously presented) The semiconductor package of claim 26 wherein the first metal layer comprises copper, the second metal layer comprises nickel and the third metal layer comprises gold.

29. (currently amended) The semiconductor package of claim 26 wherein the substrate comprises a material selected from the group consisting of ~~bismaleimide-trizine (BT),~~ organic polymer materials, epoxy resins, and polyimide resins.

Claims 30-57 (canceled)

58. (currently amended) An electronic assembly comprising:

a supporting substrate comprising a plurality of electrodes;

at least one semiconductor package on the supporting substrate comprising:

a substrate comprising a plurality of bonding sites, each bonding site comprising an electrically conductive, bondable metal;

a semiconductor die on the substrate comprising a plurality of bond pads in electrical communication with the bonding sites; and

a plurality of external contacts on the bonding sites bonded to the electrodes on the substrate, each external contact comprising a multi layered metal bump including a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing outer layer on the second metal layer.

59. (previously presented) The assembly of claim 58 wherein the substrate and the package are configured as a multi chip module.

60. (previously presented) The assembly of claim 58 wherein the first metal layer comprises copper, the second metal layer comprises nickel, and the non-oxidizing outer layer comprises gold.

61. (previously presented) The assembly of claim 58 wherein the package further comprises a plurality of die contacts on the substrate in electrical communication with the external contacts, the die contacts comprising multi layer metal bumps bonded to the bond pads on the die.

62. (currently amended) An electronic assembly comprising:

a supporting substrate comprising a plurality of electrodes; and

a semiconductor package comprising a substrate having a first side and an opposing second side, a plurality of die contacts on the ~~substrate~~ first side comprising first multi layered metal bumps having generally planar first tip portions, a plurality of bonding sites on the second side in electrical communication with the die contacts comprising an electrically conductive bondable metal, a semiconductor die bonded to the die contacts in a flip chip configuration, and a plurality of external contacts on the ~~substrate~~ bonding sites ~~in electrical communication with the die contacts~~ comprising second multi layer metal bumps having generally planar second tip portions bonded to the electrodes.

63. (previously presented) The assembly of claim 62 wherein each die contact comprise a copper layer, a nickel layer and a gold layer.

64. (previously presented) The assembly of claim 62 wherein each external contact comprise a copper layer, a nickel layer and a gold layer.